AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An apparatus for simulating ~~modeling~~ an anti-resonance circuit of a section of a microprocessor, comprising:

   a processor;

   memory;

   instructions residing the memory and executable on the processor, the instruction for representing:

   a simulated load that models a load of ~~model that simulates~~ the anti-resonance circuit;

   a simulated transistor that ~~simulates~~ models at least one high-[[ ]]frequency capacitance of the anti-resonance circuit ~~capacitor~~, wherein the simulated transistor is connected in parallel with the simulated load ~~model~~; and

   a simulated capacitor that ~~simulates~~ models an intrinsic capacitance of ~~a~~ the section of the microprocessor, wherein the simulated capacitor is connected in parallel with the simulated load ~~model~~.

2. (Currently Amended) The apparatus of claim 1, wherein the simulated load ~~model~~ is ~~simulates the anti-resonance circuit with~~ a simulated resistor.

3. (Currently Amended) The apparatus of claim 2, wherein the simulated resistor is a simulated voltage-[[ ]]controlled resistor.

4. (Curerntly Amended) The apparatus of claim 1, wherein ~~the load model simulates~~ the anti-resonance circuit is simulated in synchronization with a simulated clock cycle.

5. (Cancelled)

6. (Currently Amended) The apparatus of claim 4, wherein simulation of ~~the load model begins to simulate~~ the anti-resonance circuit begins on a leading edge of the simulated clock cycle.

7. (Cancelled)

8. (Currently Amended) A method for ~~modeling~~ simulating an anti-resonance circuit of a section of a microprocessor, comprising:

simulating ~~modeling~~ a load ~~to generate a simulation~~ of ~~an~~ the anti-resonance circuit;

simulating at least one high frequency capacitance of the anti-resonance circuit ~~capacitor~~ in parallel with the simulated load ~~model~~; and

simulating ~~a section of the microprocessor's~~an intrinsic capacitance in parallel with the simulated load ~~model~~.

9. (Currently Amended) The method of claim 8, wherein the load is simulated ~~modeled~~ with a simulated resistor.

10. (Currently Amended) The method of claim 9, wherein the simulated resistor is a simulated voltage[[ ]]-controlled resistor.

11. (Currently Amended) The method of claim 8, wherein ~~the~~ simulation of the anti-resonance circuit is synchronized with a simulated clock cycle.

12. (Cancelled)

13. (Currently Amended) The method of claim 11, wherein ~~the~~ simulation of the anti-resonance circuit begins on ~~the~~ a leading edge of the simulated clock cycle.

14. (New) An apparatus for simulating an anti-resonance circuit of a section of a microprocessor, comprising:

a processor;

memory; and

instructions residing in the memory and executable by the processor, the instructions to:

simulate a load of the anti-resonance circuit with a simulated resistor;

simulate a high-frequency capacitance of the anti-resonance circuit with a simulated transistor connected in parallel with the simulated resistor; and

simulate an intrinsic capacitance of the section of the microprocessor with a simulated capacitor connected in parallel with the simulated resistor.

15. (New) The apparatus of claim 14, wherein the simulated resistor is a simulated voltage controlled resistor.

16. (New) The apparatus of claim 14, wherein the anti-resonance circuit is simulated in synchronization with a simulated clock cycle.

17. (New) The apparatus of claim 14, wherein the simulation of the anti-resonance circuit begins on a leading edge of the simulated clock cycle.